UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,174	09/08/2003	Evan Cho	JCLA10514	3340

23900 7590 01/12/2006

J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,174	CHO ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 8-11 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Scheffer et al. (US 5,459,495).

Regarding claim 1, Scheffer et al. disclose a double waveform method for driving a transmission line originally at an initial voltage to a final voltage (Figure 3A and Figure 3A and column 5, lines 7-35.), comprising the steps of:

finding a first voltage, a second voltage, a first voltage maintenance period and a second voltage maintenance period according to the initial voltage and the final voltage (Figure 3A and column 5, lines 7-35. The examiner interprets that S+D is a first voltage, S-D is a second voltage, f is a first voltage maintenance period and 1-f is a second voltage maintenance period, where f corresponds to the first S+D voltage and 1-f corresponds to the S-D voltage, and that these values are found corresponding to the gray level voltage, i.e. final voltage, needed to be achieved from the initial voltage.);

putting up the first voltage on the transmission line for a time period equal

to the first voltage maintenance period (Figure 3A and column 5, lines 7-35. The examiner interprets that the column signal with S+D for the time period of f is put on the display panel which acts as a transmission line.);

putting up the second voltage on the transmission line for a time period equal to the second voltage maintenance period (Figure 3A and column 5, lines 7-35. The examiner interprets that the column signal with S-D for the time period of 1-f is put on the display panel which acts as a transmission line.); and

putting up the final voltage on the transmission line (Figure 3A and column 5, lines 7-35. The examine interprets that since the RMS voltage averaged over one frame period is intermediate between the first and second voltages, that this is the final voltage and is put on the display panel column line, which acts as a transmission line.).

Regarding claim 2, Scheffer et al. disclose the method of claim 1, wherein either the first voltage or the second voltage is higher than the final voltage when the final voltage is higher than the initial voltage (Figure 3A. Since the final voltage is intermediate between S+D and S-D, S+D would be higher than the final voltage and the final voltage would be higher than the initial voltage, shown in the figure as –D.).

Regarding claim 3, Scheffer et al. disclose the method of claim 1, wherein either the first voltage or the second voltage is lower than the final voltage when the final voltage is smaller than the initial voltage (It is inherent for a flat panel display to use alternating voltage between frame periods, which in this case would flip the waveform

shown in Figure 3A about the X-axis which would cause the flipped voltage of S+D lower than the final voltage which would still be intermediate between S+D and S-D, and the initial voltage would be larger than the final voltage.).

Regarding claim 4, Scheffer et al. disclose the method of claim 1, wherein the transmission line includes the transmission line on a flat display panel (Figure 1).

Regarding claim 8, Scheffer et al. disclose a double waveform method for driving a signal through a transmission line at a first initial voltage (Figure 3A and Figure 3A and column 5, lines 7-35.), comprising the steps of:

putting a first voltage on the transmission line for a first period of time (Figure 3A and column 5, lines 7-35. The examiner interprets that the column signal with S+D for the time period of f is put on the display panel which acts as a transmission line.);

putting a second voltage on the transmission line for a second period of time (Figure 3A and column 5, lines 7-35. The examiner interprets that the column signal with S-D for the time period of 1-f is put on the display panel which acts as a transmission line.); and

putting a final voltage on the transmission line (Figure 3A and column 5, lines 7-35. The examine interprets that since the RMS voltage averaged over one frame period is intermediate between the first and second voltages, that this is the final voltage and is put on the display panel column line, which acts as a transmission line.).

Regarding claim 9, Scheffer et al. disclose the method of claim 8, wherein either the first voltage or the second voltage is higher than the final voltage when the final voltage is higher than the initial voltage (Figure 3A. Since the final voltage is intermediate between S+D and S-D, S+D would be higher than the final voltage and the final voltage would be higher than the initial voltage, shown in the figure as –D.).

Regarding claim 10, Scheffer et al. disclose the method of claim 8, wherein either the first voltage or the second voltage is lower than the final voltage when the final voltage is lower than the initial voltage (It is inherent for a flat panel display to use alternating voltage between frame periods, which in this case would flip the waveform shown in Figure 3A about the X-axis which would cause the flipped voltage of S+D lower than the final voltage which would still be intermediate between S+D and S-D, and the initial voltage would be larger than the final voltage.).

Regarding claim 11, Scheffer et al. disclose the method of claim 8, wherein the transmission line includes the transmission lines on a flat display panel (Figure 1).

Regarding claim 15, Scheffer et al. disclose a double waveform method for driving a transmission line at an initial voltage (Figure 3A and Figure 3A and column 5, lines 7-35.), comprising the steps of:

finding a first maintenance period for a first voltage according to the initial voltage and the final voltage and putting the first voltage on the transmission line for a

time period equal to the first maintenance period (Figure 3A and column 5, lines 7-35. The examiner interprets that f is a first voltage maintenance period and 1-f is a second voltage maintenance period, where f corresponds to the first S+D voltage and that this value is found corresponding to the gray level voltage, i.e. final voltage, needed to be achieved from the initial voltage.);

finding a second maintenance period for a second voltage according to the initial voltage and the final voltage and putting the second voltage on the transmission line for a time period equal to the second maintenance period (Figure 3A and column 5, lines 7-35. The examiner interprets that 1-f is a second voltage maintenance period, where 1-f corresponds to the S-D voltage, and that this value is found corresponding to the gray level voltage, i.e. final voltage, needed to be achieved from the initial value.); and

putting the final voltage on the transmission line (Figure 3A and column 5, lines 7-35. The examine interprets that since the RMS voltage averaged over one frame period is intermediate between the first and second voltages, that this is the final voltage and is put on the display panel column line, which acts as a transmission line.);

wherein the first voltage and the second voltage cannot be both equal to the final voltage (Figure 3A and Figure 3A and column 5, lines 7-35. S-D and S+D both are not equal to the final voltage.),

the first voltage and the second voltage cannot be both equal to the initial voltage (Figure 3A and Figure 3A and column 5, lines 7-35. S-D and S+D are both not equal to the initial voltage.)

and the first maintenance period and the second maintenance period cannot be both zero (Figure 3A and Figure 3A and column 5, lines 7-35. f and 1-f are both not zero.).

Regarding claim 16, Scheffer et al. disclose the method of claim 15, wherein either the first voltage or the second voltage is higher than the final voltage when the final voltage is higher than the initial voltage (Figure 3A. Since the final voltage is intermediate between S+D and S-D, S+D would be higher than the final voltage and the final voltage would be higher than the initial voltage, shown in the figure as –D.).

Regarding claim 17, Scheffer et al. dsiclose the method of claim 15, wherein either the first voltage or the second voltage is lower than the final voltage when the final voltage is lower than the initial voltage (It is inherent for a flat panel display to use alternating voltage between frame periods, which in this case would flip the waveform shown in Figure 3A about the X-axis which would cause the flipped voltage of S+D lower than the final voltage which would still be intermediate between S+D and S-D, and the initial voltage would be larger than the final voltage.).

Regarding claim 18, Scheffer et al. disclose the method of claim 15, wherein the transmission line includes the transmission lines on a flat display panel (Figure 1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 5-7, 12-14 and19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scheffer et al. (US 5,459,495) in view of Chang et al. (US 6,611,247).

Regarding claim 5, Scheffer et al. disclose the method of claim 1.

Scheffer et al. fail to teach wherein a buffer unit can be deployed to drive the transmission line.

Chang et al. disclose wherein a buffer unit can be deployed to drive the transmission line (Figures 5 and 8. The examiner interprets that it is inherent for a liquid

crystal display panel to have operation amplifiers between the data driver and the display panel, which act as buffer units.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the buffer units as taught by Chang et al. with the flat panel display method taught by Scheffer et al. in order to help facilitate the multi-level signaling used for transferring display data needed for image display on a display panel.

Regarding claim 6, Scheffer et al. and Chang et al. disclose the method of claim 5. Chang et al. also disclose wherein the buffer unit is coupled to a digital-to-analogue converter (Figures 5 and 8. The DAC would be connected to the output buffer located between the data driver and the display panel.).

Regarding claim 7, Scheffer et al. and Chang et al. disclose the method of claim 6. Chang et al. also disclose wherein the digital-to-analogue converter is coupled to a waveform encoder (Figures 5 and 7. The multi-level encoder 74 is located in item 70 which is coupled to item 80 containing the DAC.).

Regarding claim 12, Scheffer et al. disclose the method of claim 8.

Scheffer et al. fail to teach wherein a buffer unit can be deployed to drive the transmission line.

Chang et al. disclose wherein a buffer unit can be deployed to drive the transmission line (Figures 5 and 8. The examiner interprets that it is inherent for a liquid crystal display panel to have operation amplifiers between the data driver and the display panel, which act as buffer units.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the buffer units as taught by Chang et al. with the flat panel display method taught by Scheffer et al. in order to help facilitate the multi-level signaling used for transferring display data needed for image display on a display panel.

Regarding claim 13, Scheffer et al. and Chang et al. disclose the method of claim 12. Chang et al. also disclose wherein the buffer unit is coupled to a digital-to-analogue converter (Figures 5 and 8. The DAC would be connected to the output buffer located between the data driver and the display panel.).

Regarding claim 14, Scheffer et al. and Chang et al. disclose the method of claim 13. Chang et al. also disclose wherein the digital-to-analogue converter is coupled to a waveform encoder (Figures 5 and 7. The multi-level encoder 74 is located in item 70 which is coupled to item 80 containing the DAC.).

Regarding claim 19, Scheffer et al. disclose the method of claim 15.

Scheffer et al. fail to teach wherein a buffer unit can be deployed to drive the transmission line.

Chang et al. disclose wherein a buffer unit can be deployed to drive the transmission line (Figures 5 and 8. The examiner interprets that it is inherent for a liquid crystal display panel to have operation amplifiers between the data driver and the display panel, which act as buffer units.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the buffer units as taught by Chang et al. with the flat panel display method taught by Scheffer et al. in order to help facilitate the multi-level signaling used for transferring display data needed for image display on a display panel.

Regarding claim 20, Scheffer et al. and Chang et al. disclose the method of claim 19. Chang et al. also disclose wherein the buffer unit is coupled to a digital-to-analogue converter (Figures 5 and 8. The DAC would be connected to the output buffer located between the data driver and the display panel.).

Regarding claim 21, Scheffer et al. and Chang et al. disclose the method of claim 20. Chang et al. also disclose wherein the digital-to-analogue converter is coupled to a waveform encoder (Figures 5 and 7. The multi-level encoder 74 is located in item 70 which is coupled to item 80 containing the DAC.).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Koshoubu et al. (US 5,966,111) discloses a double waveform method for a matrix type liquid crystal display device.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

27 December 2005

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER